1

Patent claims

- 1. Method for switching a semiconductor power switch (S1, S2), characterized in that the resistance of the switching path (E-A) of the semiconductor power switch (S1, S2) is controlled via a control input (s, g) by a control voltage (Vst) and/or a control current depending on the chip temperature (Tlist, T2ist) to such an extent that the chip temperature (Tlist, T2ist) of the power switch (S1, S2) is kept at a predetermined nominal temperature Tsoll, in which case, when the nominal temperature (Tsoll) is reached, the resistance of the switching path (E-A) is increased.
- 2. Device for implementing the method according to Claim 1, especially for actuating a semiconductor power switch (S1, S2) arranged between two energy storage devices (C1, DLC, B36) in a wiring system of the vehicle equipped with an integrated starter generator (ISG),
- in which the power switch (S1, S2) which can be controlled by means of a control voltage Vst so that it conducts or does not conduct is embodied as a transfer gate (TG)
- which features two transistors (Q1, Q2) or groups of transistors connected in series of which, in the off-state of the power switch (S1, S2), at least one is blocked, and characterized in that
- each transistor (Q1, Q2) or each group of transistors is assigned at least one diode (DT1, DT2) for recording the chip temperature (Tlist, T2ist),

for generating the control voltage (Vst), a charge pump (LP) is provided by means of which the transistors (Q1, Q2) of the

power switch (S1, S2), in the conductive state, are in each case only controlled to such an extent that the chip temperature (T1ist, T2ist) of each transistor (Q1, Q2) of the power switch (S1, S2) is kept to a predetermined required temperature Tsoll, and

- a temperature recording unit is provided in which the comparison of the chip temperatures with the required value is undertaken, and which delivers an enable signal (En) assigned to this comparison for the charge pump (LP), with the resistance of the switching path (E-A) being increased when the required temperature is reached.
- 3. Device according to claim 2, characterized in that a transistor (Q3) is assigned to the transfer gate (S1, S2, TG), of which the collector-emitter path is arranged between the interconnected gate connections (g) and the interconnected source connections (s) of two transistors (Q1, Q2) or groups of transistors connected in series, and which can be shifted by means of an external signal (Dis) to the conductive state in order to rapidly make the transfer gate (TG) non-conductive.
- 4. Device according to claim 2 or 3, characterized in that the temperature recording unit features at least one series circuit at the poles (+5v, GND) of a voltage source, consisting of the diode (DT1, DT2) assigned to it and a resistor (R7, R8) for each transistor (Q1, Q2) or for each group of transistors, the connection point between resistor (R7, R8) and diode (DT1, DT2) at which a voltage (VTlist, VT2ist) assigned to the chip temperature (Tlist, T2ist) can be tapped, is connected in each case to the input of a comparator (K1, K2), at another input of the comparator (K1, K2) a nominal voltage (Vtsoll) assigned to the predetermined nominal temperature (Tsoll) is applied,

the comparator (K1, K2) performs the comparison of the voltage (VT1ist, VT2ist) assigned to the chip temperature (T1ist, T2ist) with the nominal voltage (VTsoll) assigned to the predetermined nominal temperature (Tsoll), the outputs of all comparators (K1, K2) are connected to the inputs of a first logic element (NAND), the output of the first logic element (NAND) is connected to the input of a second logic element (NOR) of which an ON/OFF signal (Dis) is fed to the other input, and the output signal of the second logic element (NOR) is fed to the gate oscillator (U1 to U4) of the charge pump (LP) as an enable signal (En).

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